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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
09/654,943	09/01/2000	Seung Kuk Ahn	8733-294-00	7898	
30827	7590 01/12/2005		EXAM	INER	
MCKENNA LONG & ALDRIDGE LLP			KOVALICK, VINCENT E		
1900 K STREET, NW WASHINGTON, DC 20006			ART UNIT	PAPER NUMBER	
	,		2673		

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Applic	ation No.	Applicant(s)			
Office Action Summary		09/654	1,943	AHN, SEUNG KUK			
		Exami	ner	Art Unit			
		Vincen	t E Kovalick	2673			
Period fo	- The MAILING DATE of this communi or Reply	cation appears on	the cover sheet with ti	ne correspondence a	ddress		
THE - Exter after - If the - If NC - Failu Any I	ORTENED STATUTORY PERIOD FOR MAILING DATE OF THIS COMMUNION IN THE PROPERTY OF THIS COMMUNION IN THE PROPERTY OF THE PROPERTY	CATION. of 37 CFR 1.136(a). In no unication. of days, a reply within the tutory period will apply an will, by statute, cause the	o event, however, may a reply to statutory minimum of thirty (30) d will expire SIX (6) MONTHS application to become ABAND	be timely filed days will be considered time from the mailing date of this ONED (35 U.S.C. § 133).			
Status							
1)🖂	Responsive to communication(s) file	d on					
2a)□	This action is FINAL .	b)⊠ This action i	s non-final.	•			
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Dispositi	on of Claims						
5)□ 6)⊠ 7)⊠	 Claim(s) 1-20 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. Claim(s) is/are allowed. Claim(s) 1-6 and 10-17 is/are rejected. Claim(s) 7-9 and 18-20 is/are objected to. 						
Applicati	on Papers						
9)[The specification is objected to by the	Examiner.					
10)	10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11)	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority u	ınder 35 U.S.C. § 119						
12)⊠ . a)[Acknowledgment is made of a claim f All b) Some * c) None of: 1. Certified copies of the priority of 3. Copies of the certified copies of application from the Internation of the attached detailed Office action	documents have be documents have be of the priority documents from the priority docume	een received. een received in Applic ments have been rece Rule 17.2(a)).	cation No eived in this Nationa	l Stage		
Attachmen	t(e)						
	e of References Cited (PTO-892)		4) Interview Summ	nary (PTO-413)			
2) Notic 3) Inform	e of Draftsperson's Patent Drawing Review (P nation Disclosure Statement(s) (PTO-1449 or f r No(s)/Mail Date		Paper No(s)/Ma		⁻ O-152)		

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DETAILED ACTION

Response to Reply Under 37 C.F.R. 1.111

1. This Office Action is in response to Applicant's Reply Under 37 C.F.R. 1.lll, dated August 2, 2004, in response to USPTO Office Action dated February 3, 2004.

Regarding claims 1, 5, 11 and 16, Applicant's arguments filed August 2, 2004 have been fully considered but they are not persuasive.

Relative to claims 1, 5, 11 and 16, Applicant argues/remarks Hirakata (USP 6,496,172) fails to teach "allowing the adjacent pixels in a gate line direction within the pixel block to respond to data signals having th same polarity; and allowing the pixels within the other pixel areas except for the pixel lock to respond to data signals having a polarity contrary to the adjacent pixels at the left an right sides thereof".

Hirakata in Fig. 17A teaches the polarity pattern as taught in claims 1, 5, 11 and 16.

Regarding Applicant's argument/remarks relative to claims 6, and 17; Applicant is correct, the Morita reference (6,628,274) does not qualify as valid prior art in that filing date of the Morita (March 2, 2000) comes after the priority date (September 4, 1999) of the instant invention. The Morita prior art is herewith replaced with prior art Okumura et al. (USP 5,739,804) with a file date of March 9, 1995 as indicated in item 4 hereinbelow.

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Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 3. Claims 1-5, 11 and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirakata (USP 6,496,172).

Relative to claims 1, 5, 11 and 16, Hirakata teaches a liquid crystal display device, active matrix type liquid crystal display device, and method of driving the same (col. 5, lines 41-67; col. 6, lines 1-67 and col. 7, lines 1-16); Hirakata further teaches an apparatus and method for driving a liquid crystal panel having pixels arranged at each intersection between gate lines and data lines in a matrix type in an inversion system, comprising: first signal supplying means for setting at least one pixel block each of which includes at least two data lines within the liquid crystal panel to apply data signals having the same polarity to the adjacent pixels in a gate line direction within the pixel block; and second signal supplying means for applying data signals having a polarity contrary to the adjacent pixels at the left and right sides thereof to the pixels within the other pixel areas except for the pixel block area (Figs. 17A).

Regarding claim 2, Hirakata teaches driving a liquid crystal panel wherein the pixel block is positioned at a boundary portion between column drivers (col. 16, lines 54-59 and Fig. 17A)

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As to claim 3, Hirakata teaches driving a liquid crystal panel wherein the pixel block includes at least two data lines to which a data is applied form the same column diver (col. 16, lines 45-53 and Fig. 17A).

Relative to claims 4 and 15, Hirakata **teaches** driving a liquid crystal panel wherein all the pixels within the liquid crystal panel responds to the data signals having a polarity inverted every frame (col. 3, lines 22-25).

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata as applied to claims 5 and 16 respectively in item 3 hereinabove, and further in view of Okumura et al. (USP 5,739,804).

Regarding claims 6 ands 17, Hirakata **does not teach** a liquid crystal panel comprising line-inversion control means for controlling the first signal supplying means to apply the data signals having the same polarity to the adjacent pixels in the gate line direction; and dot-inversion control means for controlling the second signal supplying means to apply the data signals having a polarity contrary to the pixels at the left and right sides thereof.

Hirakata teaches a liquid crystal display device with no flicker and with a bright display by using a frame inversion driving technique.

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Okumura et al. teaches a liquid crystal display device in which a period other than an image display prior is extended (col. 7, lines 15-67 and col. 8, lines 1-65); Okumura et al. further teaches a liquid crystal panel comprising line-inversion control means for controlling the first signal supplying means to apply the data signals having the same polarity to the adjacent pixels in the gate line direction; and dot-inversion control means for controlling the second signal supplying means to apply the data signals having a polarity contrary to the pixels at the left and right sides thereof (col. 1, lines 53-62).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hirakata the feature as taught by Okumura et al. in order to optimize the drive device output.

6. Claims 10, 12, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirakata as applied to claims 2 and 11 respectively in item 3 hereinabove, and further in view of Jeong et al. (USP 6,271,816).

Regarding claims 10 and 13, Hirakata does not teach a method wherein data lines within a least one first plurality of consecutively arranged data lines are connected to adjacent column drivers. Hirakata teaches a liquid crystal display device with no flicker and with a bright display by using a frame inversion driving technique.

Jeong teaches a power saving circuit and method for driving an active matrix display (col. 3, lines 62-67 and col. 4, lines 1-7); Jeong et al. further teaches teach a method wherein data lines within a least one first plurality of consecutively arranged data lines are connected to adjacent column drivers (col. 2, lines 60-67; col. 5, lines 10-23 and col. 6, lines 49-62).

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It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Hirakata the feature as taught by Jeong et al. in order to provide the means to significantly reduce the power needed by the column drive circuit to drive voltages of alternating polarity onto the column electrodes, in this way significant power is saved in both the pixel inversion and the row inversion schemes (Jeong et al. col. 3, lines 66-67 and col. 4, lines 1-3).

Relative to claims 12 and 14, Jeong et al. further **teaches** the method step of providing a plurality of column drivers for applying the video signal, wherein each column driver is connected to a plurality of consecutively arranged data lines (col. 4, lines 65-67; col. 5, lines 1-9 and Fig. 1A).

Allowable Subject Matter

- 7. Claims 7-9 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 8. Regarding claims 7 and 18, the major difference between the teachings of the prior art of record (USP 6,496,172, Hirakata; USP 5,739,804, Okumura et al. and USP 6,271,816, Jeong et al.) and that of the instant invention is that said prior art of record **does not teach** an apparatus for driving a liquid crystal panel wherein the first and second signal supplying means comprises at least two signal inverters for responding to control signals applied from the line inversion control means and the dot-inversion control means to invert phases of input data signals.

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Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,559,822	Okuzono
U. S. Patent No.	6,400,350	Nishimura et al.
U.S. Patent No.	6 327 008	Fujivoshi

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Responses

10. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020.

The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent E. Kovalick

January 3, 2005

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINE

TENTION PATENT EXAMINED